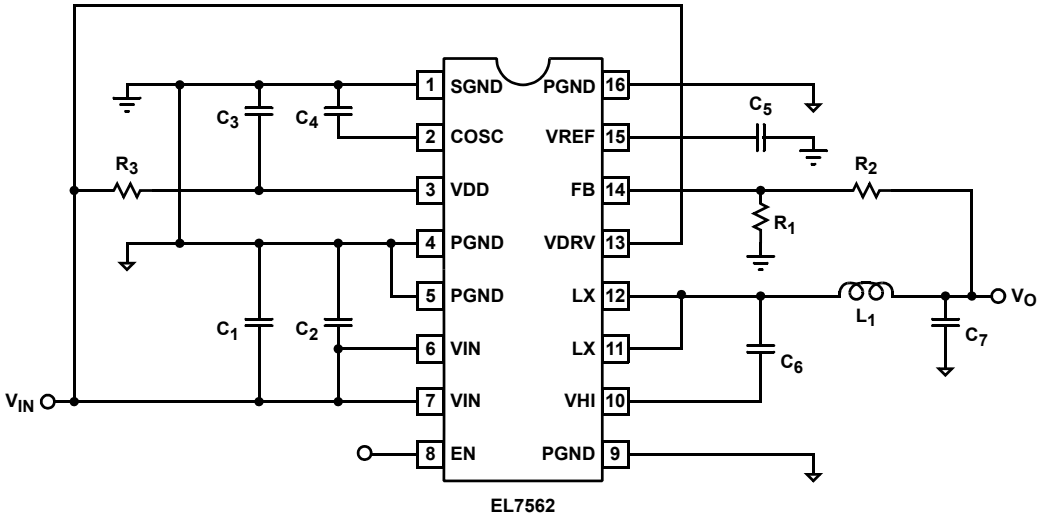
élantec

The EL7562 is a Buck (Step Down) DC:DC controller with integrated synchronous MOSFETs in a 16-pin QSOP package. With very few external components, a 2A step-down DC:DC converter can be very easily built, resulting in saved board space (0.5in^2), minimal design effort, and improved design time.

There are 2 demo boards, one for nominal 5V input and another for 3.3V input. This document outlines the design consideration and lists the bill of materials and the layout. Please also refer to the advanced data sheet of EL7562 for detailed applications of the features.

EL7562 Demo Board Circuit Schematic for V_{IN} = 5V Application

$$V_O = 0.985 \times \left(1 + \frac{R_2}{R_1}\right)$$

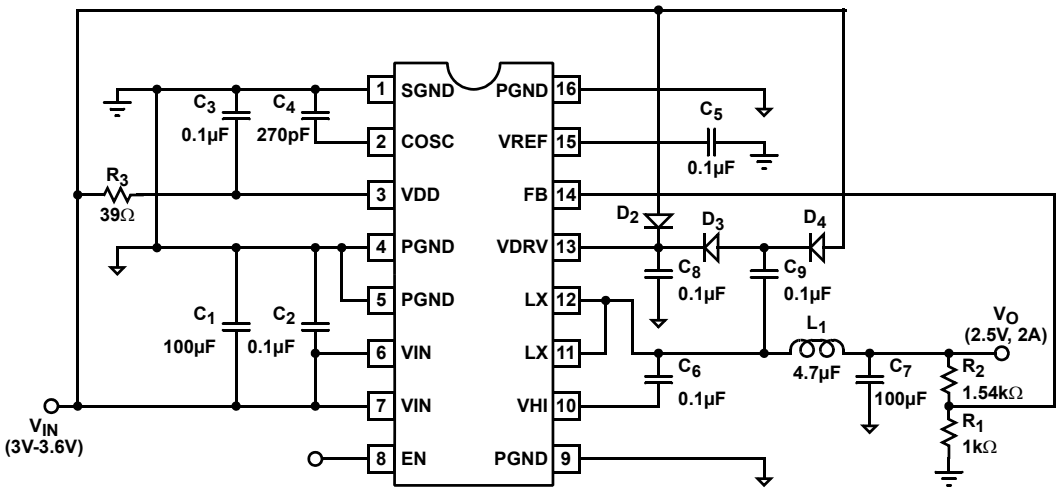


EL7562 Demo Board Bill of Material V_{IN} = 5V, V_{OUT} = 3.3V

REFERENCE DESIGNATION	VALUE	MANUFACTURER	MANUFACTURER'S PHONE NUMBER	PART NUMBER
C1	100µF	Sprague	207-324-4140	293D107X0010D2
C2, C3, C5, C6	0.1µF, 0603	Any		
C4	270pF, 5%, 0603	Any		
C7	100µF	Sprague	207-324-4140	293D107X0010D2
L1	4.7µH	Coilcraft	847-639-6400	D01813472HC
R1	1kΩ, 0603	Any		
R2	2370Ω, 0603	Any		
R3	39Ω, 0603	Any		

EL7562 Demo Board Circuit Schematic for V_{IN} = 3.3V Application

$$V_O = 0.975 \times \left(1 + \frac{R_2}{R_1}\right)$$



EL7562 Demo Board Bill of Material V_{IN} = 3.3V, V_{OUT} = 2.5V

REFERENCE DESIGNATION	VALUE	MANUFACTURER	MANUFACTURER'S PHONE NUMBER	PART NUMBER
C1	100µF	Sprague	207-324-4140	293D107X0010D2
C2, C3, C5, C6, C8, C9	0.1µF, 0603	Any		
C4	270pF, 5%, 0603	Any		
C7	100µF	Sprague	207-324-4140	293D107X0010D2
L1	4.7µH	Coilcraft	847-639-6400	D01813472HC
R1	1kΩ, 0603	Any		
R2	1.54kΩ, 0603	Any		
R3	39Ω, 0603	Any		
D2, D3/4	Bat54S	Vishay Telefunken	402-563-6863	Bat54S

Design Considerations

Choosing the Component Values

The following requirements are specified for a DC:DC converter:

- Input voltage range: V_{IN} = 4.5V-5.5V
- Output voltage: V_O = 3.3V
- Max output voltage ripple: ΔV_O = 50mV
- Output max current: I_O = 2A

The following steps briefly outline the steps to choose components.

1. Choose the feedback resister divider.

   The output voltage is decided by:

   $$V_{OUT} = 0.985 \times \left(1 + \frac{R_2}{R_1}\right)$$

   For V_{IN} = 5V

   $$V_{OUT} = 0.975 \times \left(1 + \frac{R_2}{R_1}\right)$$

   For V_{IN} = 3.3V

2. Choose the converter switching frequency F_S.

   F_S, inductor L_1, output capacitor C_7, and EL7562's switching loss are closely related. many iterations (or thermal measurements) may be required before a final value can be decided.

   Please refer to the EL7562 data sheet for the F_S vs C_{OSC} curve.

3. Inductor L_1.

   The EL7562 is internally ramp-compensated. For optimal operation, the inductor current ripple should be less than 0.6A.

   If ΔI_L = 0.5A, then:

   $$L = \frac{(1 - D) \times V_O}{\Delta I_L \times F_S}$$

   where:

   $$D = \frac{V_O}{V_{IN}}$$

   Choosing L_1 = 4.7µH yields ΔI_{LMAX} = 0.56A. L_1 should also be able to handle DC current of 2A and peak current of 2.3A at temperature range.

4. Output capacitor C_7.

   ΔV_O and ΔI_L normally decide C_7 value. ΔV_O requires ESR of C_7 be less than:

   $$ESR = \frac{\Delta V_O}{\Delta I_{LMAX}} = 89m\Omega$$

   Double-check the RMS current requirement of the output capacitor:

   $$\Delta I_{C7} = \frac{\Delta I_{LMAX}}{\sqrt{12}}$$

   which is 0.16A. For a capacitor or combination of capacitors with 89mΩ parallel ESR, it is more than enough to handle this current.

5. Input capacitors C_1 and C_2.

   If all the AC current is handled by the input capacitors its RMS current is calculated as:

   $$I_{IN,rms} = \sqrt{[D \times (1 - D)]} \times I_O$$

   This gives almost 0.99A when D = D_{MAX}. Therefore a cap with 0.99A current handling capability should be chosen. However, in case some other capacitor is sharing current with it, this current requirement can be reduced.

Layout Considerations

The layout is very important for the converter to function properly. Power Ground (⏚) and Signal Ground (⏚) should be separated to ensure that the high pulse current in the Power Ground never interferes with the sensitive signals connected to Signal Ground. They should only be connected at one point (normally at the negative side of either the input or output capacitor.)

The trace connected to pin 14 (FB) is the most sensitive trace. It needs to be as short as possible and in a "quiet" place, preferably between the PGND and SGND traces.

In addition, the bypass capacitor C_3 should be as close to pins 1 and 3 as possible.

The heat of the chip is mainly dissipated through the PGND pins. Maximizing the copper area around these pins is preferable. In addition, a solid ground plane is always helpful for the EMI performance.

Demo Board Layout for V_{IN} = 5V

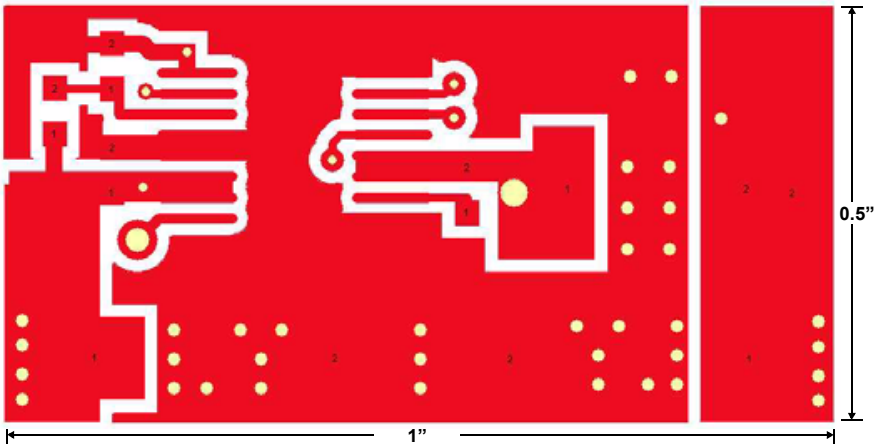


FIGURE 1. TOP LAYER

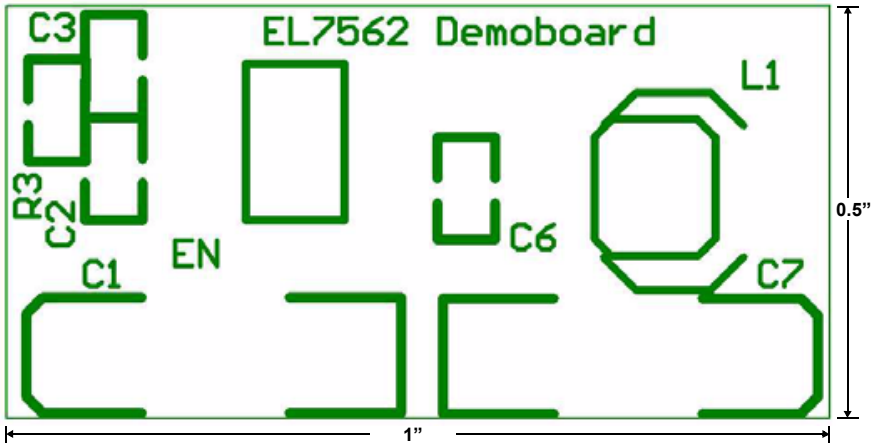


FIGURE 2. TOP SILKSCREEN

Demo Board Layout for V_{IN} = 5V (Continued)

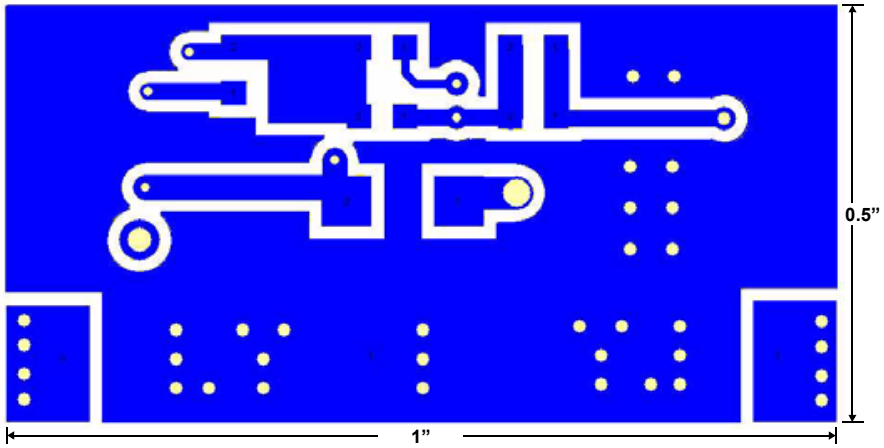


FIGURE 3. BOTTOM LAYER

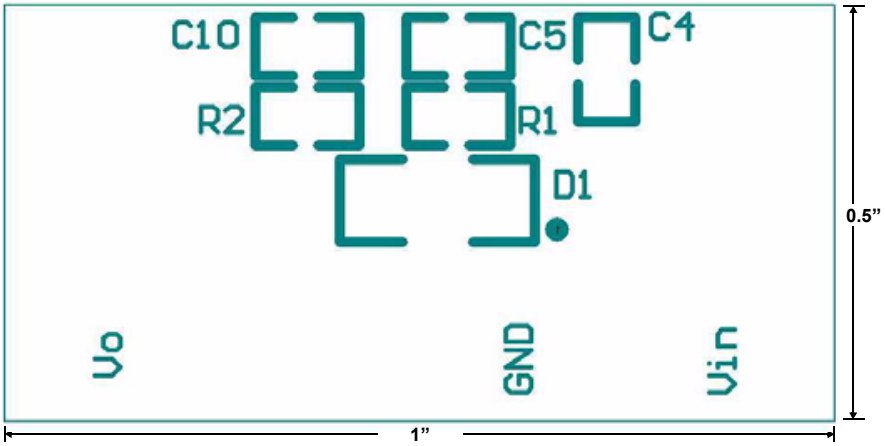


FIGURE 4. BOTTOM SILKSCREEN

Demo Board Layout for V_{IN} = 3.3V

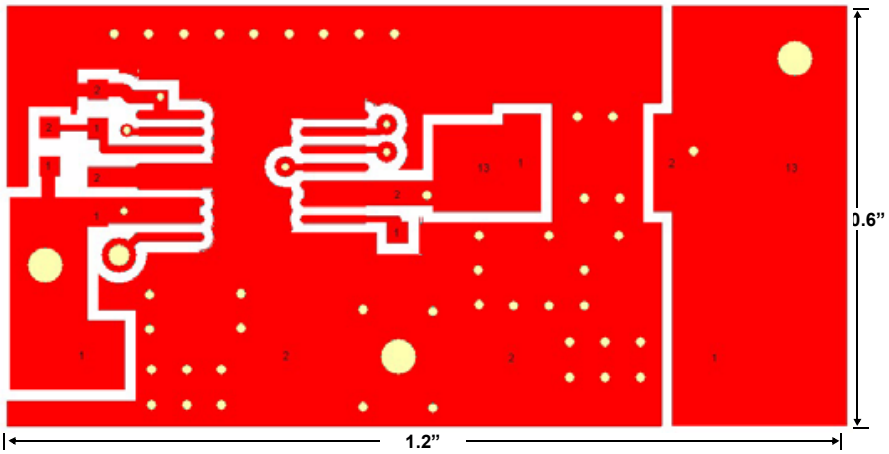


FIGURE 5. TOP LAYER

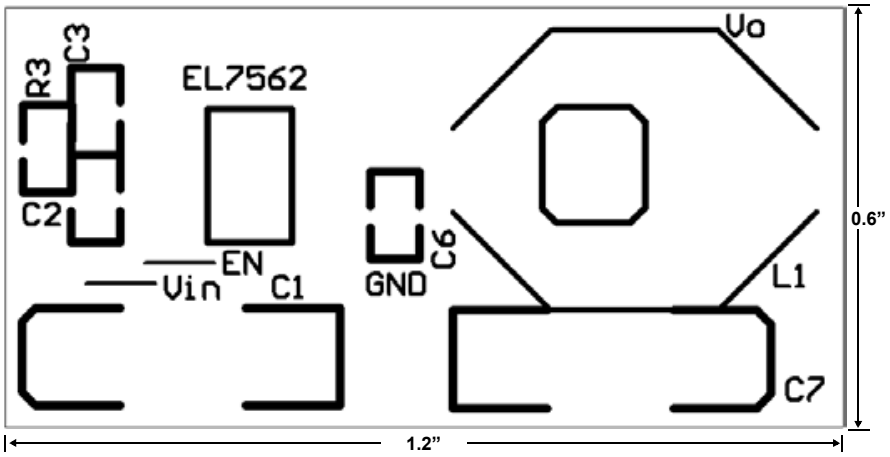


FIGURE 6. TOP SILKSCREEN

Demo Board Layout for V_{IN} = 3.3V (Continued)

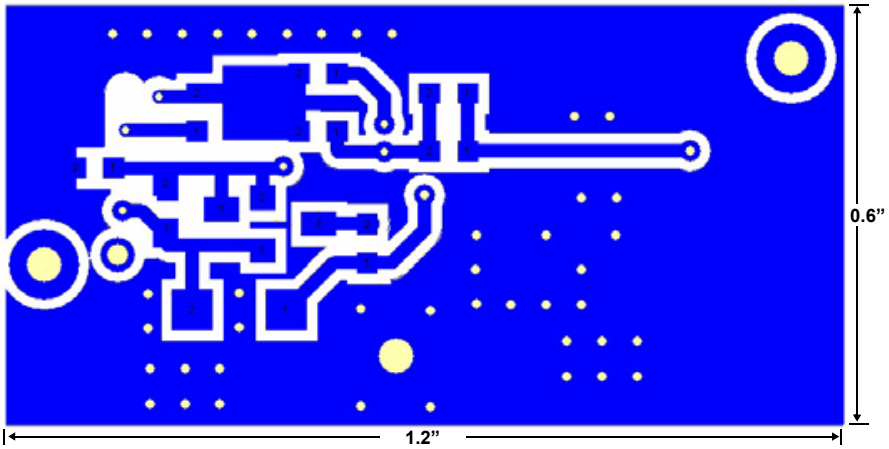


FIGURE 7. BOTTOM LAYER

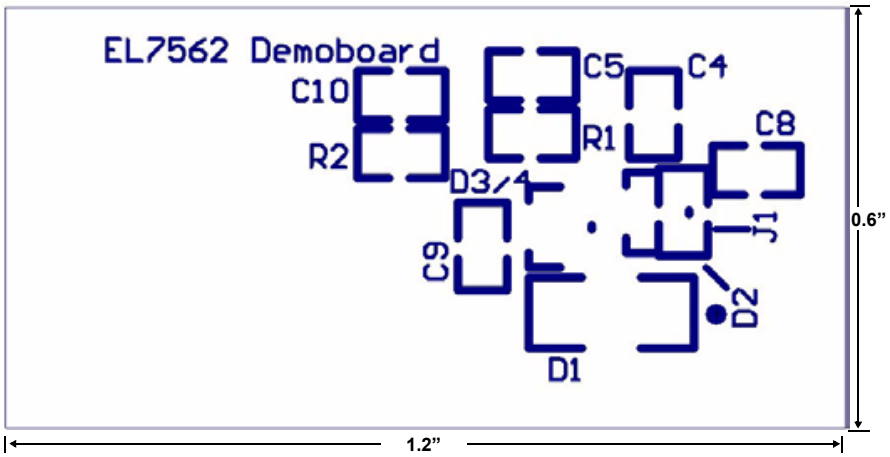


FIGURE 8. BOTTOM SILKSCREEN